This reply is submitted as a complete response to the outstanding Office Action. Reconsideration of the application in view of the above amendments and following remarks is respectfully requested.

MATTERS OF FORM

The Office Action rejects claim 2 under 35 U.S.C. § 112, second paragraph, asserting lack of antecedent basis. Applicants have amended claim 2 to obviate this rejection. Accordingly, withdrawal of this rejection is respectfully requested.

PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1 and 4-12 under 35 U.S.C. § 103(a) over Usami (U.S. Patent No. 6,205,516B1) in view of Fadavi-Ardekani (U.S. Patent No. 6,401,176). This rejection is respectfully traversed.

Applicants' independent claim 1 recites a synchronous DRAM comprising, one memory array divided into a plurality of memory blocks, mode storage units so disposed in a plurality of stages as to correspond to the memory blocks, for storing control information for defining operation modes of the memory blocks. A setting unit is provided for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. A mode selection unit is provided for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted, and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of the memory blocks in accordance with the control information stored in the mode storage unit selected.

As described in the Applicants' specification, the mode storage units independently stores control information. Thus, memory blocks are allowed to operate independently in the operation mode represented by the control information stored in the corresponding mode storage units. This arrangement eliminates the necessity for changing a setting of the mode register set whenever the operation mode is changed, as necessary in the prior art. Thus, synchronous DRAM can be used in common among a plurality of controllers requiring different operation modes. See page 6, lines 12-29, for example.

Usami discloses a method for designating a unique address data to select mode operations via mode register 35. When the address data corresponds to a memory area designated as the operation mode setting portion, specific address data indicating the desired operation mode, based on the received commands data and the specific control signal for setting the operation mode setting portion, the specific address data and the specific control signal is output. This causes the operation mode setting portion to be set with the desired operation mode. See col. 5, lines 5-12, for example. Usami utilizes a memory control circuit 5a, a memory selection circuit 20 and the control signal generator 21 to coordinate accessing of the memory. However, as stated above, the mode register areas are part of the memory map and are addressed according to the respective address in the memory map. Thus the memory and the mode is controlled by a unique address data.

In contrast, Applicants' invention utilizes a plurality of load storage units to independently provide control information for defining operation modes of the various memory blocks. Further, Applicants' invention utilizes a setting unit for setting the control information and a mode selection unit for selecting the mode storage unit.

It is readily apparent from the above, that Usami's memory control circuit 5a is not a setting unit and a mode selection unit. Further, the functions of the selection circuit 20 and the control signal generator 21 of the memory control circuit 5a are different from the function of the setting unit of Appliants' invention.

Accordingly, Applicants respectfully submit that Usami does not disclose or suggest all the claimed features of the Applicants invention. Additionally, Fadavi-Ardekani does not supply the subject matter lacking in Usami. In fact, as stated in the Office Action, Fadavi-Ardekani is applied for its disclosure of multiple processors.

Fadavi-Ardekani discloses a multiple agent system for use of a multi-ported memory 200 via an arbitrator switch 102. Each agent requests a signal to the arbitrator, which synchronizes the agent's requesting clock to the memory clock. Thus, memory can be more efficiently distributed and accessed by the independent agents.

At no point does Fadavi-Ardekani disclose or even contemplate the plurality of load storage units, a setting unit for setting the control information and a mode selection unit for selecting the mode storage unit, as discussed above lacking in Usami. In fact, since Fadavi-Ardekani is directed to an altogether different problem of the prior art, than the Applicants' invention, Applicants respectfully submit that Fadavi-Ardekani does not supply the subject matter lacking in Usami. Thus, Usami and Fadavi-Ardekani, individually or in combination, do not disclose or suggest all the claimed features of Applicants' invention.

Claims 4-12 depend from claim 1. Therefore, for at least the above reasons, Applicants respectfully request the withdrawal of this rejection.

The Office Action rejects claims 1 and 3-12 under 35 U.S.C. § 103(a) over Rao (U.S. Patent No. 6,173,356B1) in view of Usami. This rejection is respectfully

traversed.

Rao discloses a multi-port memory connected to a plurality of processors 201, each processor having their memory requests arbitrated by a memory controller 202. The memory controller 202 addresses different portions of the memory according to the designated registers in the memory controller 202. See col. 10, lines 25 - 55 and Fig. 7, for example. Accordingly, multi-processing using a common memory is facilitated.

It is readily apparent that Rao, similar to Fadavi-Ardekani, is concerned with coordinating the memory requests of different processors, and like Fadavi-Ardekani, is not concerned with the mode setting problems addressed by the Applicants' invention. Thus, Applicants respectfully submit that Rao does not supply the subject matter lacking in Usami.

Accordingly, in view of the above, Applicants respectfully submit that Usami and Rao, individually or in combination, do not disclose or suggest all the claimed features of Applicants' invention.

Claims 3-12 depend from claim 1. Therefore, for at least the above reasons, Applicants respectfully request the withdrawal of this rejection.

The Office Action rejects claims 1, 3-10 and 12 under 35 U.S.C. § 103(a) over Farrer (U.S. Patent No. 5,307,320) in view of Fadavi-Ardekani. This rejection is respectfully traversed.

Farrer discloses a memory controller for various types of DRAM configurations, having one register associated with every bank location. Each register is programmable to accommodate various DRAM bank types. See col. 2, lines 9 - 37 and col. 3, line 52 - col. 4, line 17, for example. Farrer is primarily concerned with different types of DRAM and

coordinating the correct address and control signals for the different types of DRAM. Farrer contains no discussion regarding a plurality of load storage units to independently provide control information for defining operation modes of the various memory blocks, and a setting unit for setting the control information and a mode selection unit for selecting the mode storage unit.

Accordingly, Applicants respectfully submit that Farrer does not disclose the subject matter lacking in Fadavi-Ardekani, as discussed above. Thus, Farrer and Fadavi-Ardekani, individually or in combination, do not disclose or suggest all the claimed features of Applicants' invention.

Claims 3-10 and 12 depend from claim 1. Accordingly, for at least the above reasons, Applicants respectfully request the withdrawal of this rejection.

CONCLUSION

In view of the above remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance of claims is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100021-00046.

Respectfully submitted,

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Enclosures: Marked-Up Copy of Amended Claim
Petition for Extension of Time (3 months)

MARKED-UP COPY OF AMENDED CLAIM

2. (Once Amended) A synchronous DRAM according to claim 1, wherein said plurality of memory [clocks] blocks is constituted by continuous memory cells designated by addresses.